Silicon-based CMOS devices with traditional structures are approaching fundamental physical limits. Researchers are looking for ways to continue the trend of scaling by using alternative materials such as Ge and III-V compound semiconductors that could out-perform Si-based CMOS. Although significant progress is made on InGaAs MOSFETs with ALD high-k dielectrics (Al₂O₃, HfO₂, HfAlO, and ZrO₂), GaAs MOSFETs remain a big challenge, mostly showing minuscule drain currents. In this paper, we report on the strong dependence of the electrical properties on different GaAs surface orientations. (111)A Ga polar surface is much more forgiving in terms of Fermi-level pinning for n-channel GaAs MOSFET as shown in Fig. 1, compared to (100) Ga-As non-polar surface. It might be directly related with ALD surface chemistry and could be explained by the trap neutral level model. In order to further scale down the equivalent oxide thickness (EOT) of dielectrics, the integration of ALD higher-k (LaLuO₃) on GaAs was systematically studied. The precursors lanthanum tris(N,N'-diisopropylformidinate), and lutetium tris(N,N'-diethylformamidinate) reacted with water vapor at 350 °C. The dielectric structures are shown in Fig. 2. Fig. 3 shows multi-frequency CV characteristics on n-type and p-type MOS capacitors on GaAs (100) surface with 2 nm Al₂O₃/8 nm LaLuO₃/2nm Al₂O₃ as composite dielectric (structure A in Fig. 2). The observed frequency dispersion at accumulation capacitance is comparable to that of pure ALD Al₂O₃. Meanwhile, LaLuO₃ with k = 25 to 30 provides a significant advantage in capacitance values. The work verifies the potential to integrate ALD higher-k dielectrics on III-V and deliver 1-2 nm EOT dielectrics by ALD for aggressively scaled ultimate CMOS technology.

Figure 1 I-V characteristics of an NMOSFET on GaAs (111)A surface with 8nm ALD Al₂O₃ as gate dielectric.

Figure 2 Four LaLuO₃ higher-k dielectric structures on GaAs.

Figure 3 Multi-frequency CV of p-type and n-type GaAs MOS capacitors with the process splits of as-grown and 600°C post-deposition anneal (PDA). The diameter of the capacitors is 100μm.
ALD high-\textit{k} and higher-\textit{k} integration on GaAs

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Outline

- Motivation
- Brief results on ALD $\text{Al}_2\text{O}_3$/GaAs(111)A MOSFET
- ALD Higher-$k$ LaLuO$_3$ deposition process
- ALD Higher-$k$ LaLuO$_3$ on GaAs (111)A and (100) surfaces
  --- 4 different MIS structures are used to investigate
- Summary
Motivation

1. Traditional III-V: high frequency and/or high power applications; New III-V thrust: high performance logic applications
Si based CMOS scaling is going to be end in 2015. For 22 nm technology node beyond, it requires novel channel materials such as III-V and high-k

2. The advantage of III-V as channel materials is high electron mobility.

3. Advantage of ALD high-k:
   --- commercial ALD tools are available
   --- ALD self-cleaning effect on III-V
   --- significant progress on III-V MOSFET in the past 3-5 years using ALD
   --- easy transfer to Si CMOS platform

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>strained Si</th>
<th>bulk Ge</th>
<th>GaAs</th>
<th>GaN</th>
<th>InP</th>
<th>In_{0.53}Ga_{0.47}As</th>
<th>InAs</th>
<th>InSb</th>
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<tbody>
<tr>
<td>$\mu_e$</td>
<td>400</td>
<td>1,000</td>
<td>3,900</td>
<td>8,500</td>
<td>1,250</td>
<td>5,400</td>
<td>8,000</td>
<td>20,000</td>
<td>30,000</td>
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<td>$\mu_h$</td>
<td>160</td>
<td>240</td>
<td>1,800</td>
<td>400</td>
<td>850</td>
<td>200</td>
<td>300</td>
<td>500</td>
<td>800</td>
</tr>
<tr>
<td>$E_g$ (eV)</td>
<td>1.1</td>
<td>1.1</td>
<td>0.66</td>
<td>1.42</td>
<td>3.4</td>
<td>1.35</td>
<td>0.72</td>
<td>0.36</td>
<td>0.18</td>
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</tbody>
</table>
Most of inversion GaAs NMOSFETs have minuscule drain current (< 1 mA/mm).

- F. Ren et al. Solid-State Electronics 41, 1751 (1997)
- any many others in 70s and 80s.

**New Solution:** our results on GaAs(111)A (next slide)

**Alternatives:**

1. In-rich InGaAs (see recent work by Purdue, Intel, IBM, NTHU, UCSB...)

2. Si interfacial control layer or SiH4 passivation on GaAs (see recent work by UT Austin, Intel, SUNY Albany, IBM, NUS, UT Dallas...)

**Potential issue:** narrow bandgap material, band-to-band tunneling...

**Potential issue:** additional SiO2 increases EOT, inversion mechanism unclear...
Inversion NMOSFET on GaAs(111)A with Al$_2$O$_3$

$V_{GS}$ 0~4V in steps of 0.5V
\[ I_{DS} = 3.5 \times 10^{-4} \, \mu A/\mu m \]

GaAs (100)

GaAs (111)A

$V_{GS}$ 0~4V in steps of 0.5V
\[ I_{DS} = 30 \, \mu A/\mu m \]

GaAs (111)A Ga polar
(111)A Ga polar
(100) Ga-As un-polar

Explained by an empirical model
Based on trap neutral level shift

$E_v$
GaAs (111)A
$E_c$

$E_v$
GaAs (100)

[* M. Xu et al, APL, 94, 212104, 2009]
[* W.E. Spice et al, JVST, 16(5), 1979]
Higher-$k$ on GaAs for EOT scaling

Further application limited due to the small $k$ value (8~9) of Al$_2$O$_3$

Implementation of higher-$k$ gate dielectric LaLuO$_3$ with $k=24$~26 !!!

Questions:
- How to integrate higher-$k$ LaLuO$_3$ on GaAs or III-V ?
- Is it feasible to integrate LaLuO$_3$ directly on GaAs ?
Higher-$k$ dielectric deposition process

<table>
<thead>
<tr>
<th>MO precursors</th>
<th>Oxidant</th>
<th>Bubbler temp.</th>
<th>Deposition temp.</th>
<th>La$_2$O$_3$ : Lu$_2$O$_3$</th>
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</thead>
<tbody>
<tr>
<td>La(amd)$_3$</td>
<td>DI H$_2$O</td>
<td>120$^\circ$C for La</td>
<td>350$^\circ$C</td>
<td>1:1</td>
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<tr>
<td>Lu(amd)$_3$</td>
<td></td>
<td>115$^\circ$C for Lu</td>
<td></td>
<td></td>
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</tbody>
</table>

[* provided by Y. Liu in Prof. Roy Gordon’s group at Harvard]
Requirements for higher-$k$ integration

Different MIS structures to be studied

- as-deposited
- PDA@600°C, 30s in N₂

(1) Ni Gate
2nm Al₂O₃
8nm LaLuO₃
2nm Al₂O₃
GaAs(111)A or (100)

(2) Ni Gate
8nm LaLuO₃
2nm Al₂O₃
GaAs(111)A or (100)

(3) Ni Gate
2nm Al₂O₃
8nm LaLuO₃
GaAs(111)A or (100)
C-V characteristics on p-type GaAs

- Capacitance increased after annealing due to water-adsorptive property of La-based dielectric.
- All p-type GaAs MOS CVs are “good-looking” with less frequency-dispersion at accumulation, which includes (100), (111)A with Al$_2$O$_3$, HfO$_2$, HfAlO and LLO.
- It relates with ALD “self-cleaning effect” on As$_2$O$_3$, As$_2$O$_5$,… (see Frank et al. 2005, Huang et al. 2005, Hinkle et al. 2007, and others) and lower half band-gap of GaAs has less problem.
C-V characteristics on Structure (1)

| Ni Gate | 2nm Al<sub>2</sub>O<sub>3</sub> | 8nm LaLuO<sub>3</sub> | 2nm Al<sub>2</sub>O<sub>3</sub> | GaAs(111)A or (100) |

Frequencies: 500Hz, 10KHz, 100KHz

EOT: ~3.3nm

- Frequency dispersion on (111)A is better than that on (100)
- Lower D<sub>it</sub> along upper half band-gap of GaAs(111)A
- EOT~3.3nm, k value is extracted to be ~24
C-V characteristics on Structure (2)

- Capacitance increased as expected and EOT scaled down to 2.3nm
- Exactly due to the removal of Al₂O₃ capping layer of 1nm EOT
- No additional interface layer introduced by metal/higher-\( k \) direct contact
Surprisingly, capacitance didn’t obviously increased after annealing.

Some interfacial layer may be introduced at higher-$k$/GaAs interface.

Will this extra-layer influence the interface quality?
Interface Trap Density on GaAs(111)A

- $D_{it}$ was extracted by $HF-LF$ method
- (3) almost has the same $D_{it}$ as the control sample, but has higher $D_{it}$ to the $E_C$ edge
- Surprisingly even with $Al_2O_3$ ICL, (1) has higher $D_{it}$ than (3)
Pure higher-$k$ direct on GaAs

Possible Problems:
Two interfaces shows good quality respectively, Why doesn’t it work with pure higher-$k$ direct on GaAs? Small conduction band offset ??

Further investigation needed !!!

No reasonable C-V characteristic obtained !!!
Summary

- Inversion NMOSFET is realized by integration of ALD Al₂O₃ on GaAs(111)A
- Higher-κ LaLuO₃ is first demonstrated to be integrated on GaAs
  - metal/LaLuO₃ interface quite stable
  - Al₂O₃/LaLuO₃/GaAs has comparable interface as Al₂O₃/GaAs
  - Al₂O₃/LaLuO₃/GaAs interface may introduce additional layer after PDA
- Further study on metal/LaLuO₃/GaAs is needed

We acknowledge the valuable discussions and on-going collaboration with Prof. R.M. Wallace’s group at UT Dallas. The work is partly supported by NSF, SRC FCRP MSD Center, and DoD ARO.