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Inversion-mode GaAs wave-shaped metal-oxide-semiconductor field-effect transistors (WaveFETs) are demonstrated using atomic-layer epitaxy of La$_2$O$_3$ as gate dielectric on (111)A nano-facets formed on a GaAs (100) substrate. The wave-shaped nano-facets, which are desirable for the device on-state and off-state performance, are realized by lithographic patterning and anisotropic wet etching with optimized geometry. A well-behaved 1 μm gate length GaAs WaveFET shows a maximum drain current of 64 mA/mm, a subthreshold swing of 135 mV/dec, and an I$_{ON}$/I$_{OFF}$ ratio of greater than 10$^7$. © 2015 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4913431]

GaAs has been considered to replace Si in logic applications for decades due to its high electron mobility. To achieve high on-current surface-channel inversion-mode n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) on GaAs (100) substrate is a long-time challenge. The main obstacle is the lack of high-quality, thermodynamically stable dielectric on GaAs that can match the device criteria as SiO$_2$ on Si such as a mid-gap interface trap density (D$_{it}$) around 10$^{10}$ cm$^{-2}$ eV$^{-1}$. During the past decades, tremendous efforts have been made to improve the oxide/GaAs interface with most of focus on different types of oxides and formation methods. Recent work finds that the oxide/GaAs interface quality is strongly dependent on semiconductor surface orientations. GaAs MOSFETs fabricated on (111)A surface exhibit much higher on-state current ($I_{ON}$) than other surface-orientations such as (100) and (111)B even with the same atomic-layer-deposited (ALD) oxide. More interestingly, much larger $I_{ON}$ can be achieved on GaAs (111)A substrate with single crystalline La-based oxide dielectrics by atomic-layer-epitaxy (ALE). Mid-gap $D_n$ or Fermi-level-pinning problem is significantly reduced with epitaxial La$_2$O$_3$ on GaAs (111)A surface, because the number of dangling bonds are dramatically reduced due to the nature of epitaxial oxide/semiconductor interface. However, GaAs (111)A substrate is technologically less important than the widely available GaAs (100) substrate, in particular, for the development of a manufacturable device technology.

In this letter, we demonstrate GaAs wave-shaped MOSFETs (WaveFETs) on a GaAs (100) substrate by nano-engineering to form ALE La$_2$O$_3$ on (111)A nano-facets. GaAs (111)A surface is achieved on a GaAs (100) substrate by the development of a well-controlled anisotropic wet etching process. GaAs MOSFETs are formed on wave-shaped (111)A surface channels with epitaxial La$_2$O$_3$ as dielectric. But, all devices are fabricated on GaAs (100) substrates. These devices have on-state current ($I_{ON}$) of 64 mA/mm and transconductance ($g_m$) of 32 mS/mm with sub-threshold swing (SS) around 135 mV/dec. This work opens a route to realize high-performance GaAs MOSFETs on (100) substrates potentially. The process development and deep understanding of surface chemistry on these nano-facets could also be very important for the emerging 3D III–V devices.

Figures 1(a) and 1(b) show the schematic view and cross-sectional view of a GaAs WaveFET in this work fabricated on a semi-insulating GaAs (100) substrate with an ALE high-k dielectric. The detailed process flow is described following. An HF and H$_2$O$_2$ based anisotropic wet etching process was applied to form the wave structure with Ti/Au as hard mask illustrated in Figure 2. MOSFET fabrication starts with 2-in. semi-insulating GaAs (100) substrates. As-received wafers were first degreased at room temperature by acetone for 10 min, methanol for 5 min, and isopropanol.

![Image](https://via.placeholder.com/150)

**FIG. 1.** (a) Schematic and (b) Cross-sectional view of an inversion-mode GaAs (100) WaveFET with ALE La$_2$O$_3$. 

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for 5 min, respectively. The wave patterns were defined by electron beam lithography and Ti/Au (2 nm/10 nm) were deposited by electron beam evaporation. After lift-off process, periodically patterned Ti/Au strip hard masks were formed as illustrated in Figure 2. Then, the wafers were dipped into HF (49%): H2O2 (30%) (10:129) based solution to form the wave-shaped channels for 3 s. The wet etching time depends on the design of the fin-width (W_fin) and the gap-width (W_gap) as depicted in Figure 2. W_fin, W_gap, and etching time were optimized to achieve the maximum effective length width. The (111)A surface was obtained due to the anisotropic property of the wet etching process. The realization of (111)A other than (111)B is further confirmed by the electrical properties of the fabricated devices since the Fermi level on (111)A is expected to be pinned. After removal of Ti/Au hard mask by KI solution, the wafers were quickly trans-ferred into buffered oxide etch (BOE) for 30 s and then rinsed with deionized water. The wafers were then dipped into HF:H2O2 (49%:30%) (10:129) based solution to form the wave-shaped channels for 3 s.

**FIG. 2.** Illustration of wave channel formation by anisotropic wet etching. GaAs (111)A surface on these nano-facets is achieved by anisotropic wet etching of GaAs using HF solution.

electron-beam lithography, and then BCl3/Ar inductively coupled plasma (ICP) dry etching was applied to remove the Al2O3 and HCl wet etching was applied to remove the La2O3 above metal contact area. Au/Ge/Au/Ni/Au (5 nm/12.5 nm/15 nm/9 nm/50 nm) contact was then formed followed by a 420°C RTA in N2 for 15 s. Then, Ti/Au (30 nm/60 nm) were deposited as gate electrodes and test pads. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system. The fabricated devices have gate lengths (L_g) of 1 µm, 2 µm, and 4 µm.

The illustration of anisotropic wet etch process (HF and H2O2) is shown in Fig. 3. In this process, the wave patterned direction is critical. The wave structure has to be patterned along (011) other than (011) as shown in Figure 3(a). The effect of wave pattern direction is shown by cross-sectional scanning electron microscopy (SEM) pictures in Figures 3(b) and 3(c). Hard mask strips were patterned along (011) in Figure 3(b) and along (011) in Figure 3(c). Clear (111) surface is shown in Figure 3(b), but irregular structures are formed on fabricated (111)A nano-facet. It has been proved by C-V measurement that the epitaxial La2O3/GaAs (111)A interface exhibits Dit on the order of 10^{11} cm^{-2} eV^{-1}, which is far below the Dit level of traditional amorphous oxide on GaAs (111)A surface. The lattice mismatch of La2O3 on GaAs (111)A is ~0.04%. It is evident from TEM image that a flat and sharp interface is formed even on fabricated (111)A nano-facet. This is confirmed by C-V measurement on these samples.

**FIG. 3.** (a) Schematic diagram of wave patterned orientation. (b) and (c) Cross-sectional SEM images of wave structures patterning along (011) and (011) orientations.

Well-behaved output, transfer, and trans-conductance characteristics of a 1 µm-gate-length inversion-mode GaAs WaveFET are plotted in Figure 5, showing a maximum drain current (ID_MAX) of 64 mA/mm at a gate bias (VGS) of 4 V and a drain bias (VDS) of 2 V, a maximum gm of 32 mS/mm at VDS = 2 V, and threshold voltage (V_T) of 1.32 V. SS of...
~135 mV/dec is obtained with an equivalent oxide thickness (EOT) of ~6 nm, indicating a mid-gap interface trap density of $4.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, which is simply estimated from equation SS ~ $60 \times (1+q_{Dit}/C_{ox})$ mV/dec. SS could be further improved by optimizing fabrication process and reducing EOT. It will also improve the extrinsic drain current and improving interface quality. Devices with different gate length $L_g$ (1, 2 and 4 $\mu$m) show similar SS and $V_T$ (not shown), indicating that these devices are weakly affected by short channel effects. It is also expected that these GaAs devices with a large bandgap and 3D wave structures must have better immunity to short channel effects. The GaAs WaveFET with epitaxial La$_2$O$_3$ demonstrated here has $I_{D,max}$ about 1000 $\times$ larger than that of the reference GaAs sample with amorphous Al$_2$O$_3$ dielectric (not shown) and about 10,000 $\times$ larger than that of GaAs planar MOSFET on GaAs (100) substrate with amorphous Al$_2$O$_3$. GaAs planar MOSFETs on GaAs (100) substrate with La$_2$O$_3$ as gate dielectric were also fabricated. Without the special surface orientation to form (111) hexagonal template, poor quality La$_2$O$_3$ dielectric was formed on GaAs (100) surface showing a weak gate modulation and minuscule $I_{D,max}$. Figure 5(d) summarizes the effective gate length $L_{eff}$ and the series resistance ($R_{SD}$) extracted by plotting $R_{tot}$ versus $L_g$, where $R_{tot}$ represents the total channel resistance measured from devices with various gate lengths under $V_{GS}-V_T$ from 1 to 2.5 V. $R_{SD}$ is determined to be 1.62 $\Omega$-mm, which is reasonable for implanted S/D on GaAs and can be further reduced by optimizing the processes of ion implantation and activation during S/D contact fabrication. Contact resistance ($R_C$) of 0.27 $\Omega$-mm is extracted from transmission line method. Two third of $R_{SD}$ is from the access resistance between Ohmic contacts to the channel underneath the gate. $\Delta L$, defined as the difference between the mask gate length $L_g$ and $L_{eff}$, is estimated to be $~0.36 \mu$m due to the lateral dopant diffusion caused by high-temperature activation and/or the lithographic misalignment.

In conclusion, by realizing (111)A nano-facets on (100) surface by anisotropic wet etching and a high-quality epitaxial La$_2$O$_3$/GaAs (111)A interface by ALE, we demonstrate inversion-mode GaAs WaveFETs on GaAs (100) substrates with much larger drain currents than those formed on planar GaAs (100) surface using the same dielectric process. The work opens up a way to improve the III-V device performance by nano-engineering semiconductor 3D structures and interfaces with high-k dielectric.

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